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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,820	08/30/2001	Anthony Eugene Zortea	3Com-85	9245

7265 7590 06/29/2005

MICHAELSON AND WALLACE
PARKWAY 109 OFFICE CENTER
328 NEWMAN SPRINGS RD
P O BOX 8489
RED BANK, NJ 07701

EXAMINER	
TORRES, JUAN A	
ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,820	ZORTEA, ANTHONY EUGENE	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,8,11,14,19,20,23 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,8,11,14,19,20,23 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "110d" has been used to designate the connection between master 115c to slave 120c and the connection between master 115d and slave 120d. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The modifications to the specification were received on 04/18/2005. These modifications are accepted by the Examiner.

Claim Objections

In view of the amendment filed on 04/18/2005, the Examiner withdraws claim objections of claims 1-4 of the previous Office Action.

Claim Rejections - 35 USC § 112

In view of the amendment filed on 04/18/2005, the Examiner withdraws the 35 USC § 112 rejection to claims 1-26 of the previous Office Action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-5, 8, 11, 14, 19-20, 23, 25, and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Rakib (US 6307868).

As per claim 1 Rakib discloses a bi-directional communication having plural channels, each of said channels comprising: a master connected at a near end of a channel and a slave connected at an opposite end of channel (figure 1 central unit and remote unit column 4 lines 8-20); the master comprising: (a) a transmitter coupled to channel and having a master Tx clock signal (figure 1 block 24 column 4 line 11); (b) receiver coupled to the channel and comprising (figure 1 block 70 column 4 lines 29-30): i) an analog-to-digital converter that periodically samples at a sampling time Ts (the ADC is inherit in the receiver of a data communications, because the signal is received as an analog signal and it has to be converted to digital values); ii) a clock recovery circuit that signal embedded in a signal received and generates a master Rx signal

received from the channel (figure 1 block 32 column 4 lines 34-35); iii) a metric processor connected to an output of said analog-to-digital converter that produces a metric signal reflective of amplitude differences between the received signal and allowed amplitude levels of the received signal (column 4 lines 41-46, figure 27 and figure 28 blocks 1512 and 467. Block 1512 indicates that the CU detects an amplitude error for the RU; to detect an amplitude error it will need to use a metric processor to produce the metric signal); the slave comprising: (a) a receiver coupled to the channel and comprising a clock recovery circuit for generating a Slave Rx clock from the signal received from the master (figure 1 block 42 column 4 lines 15); (b) a transmitter coupled to the channel and having a Slave Tx clock signal, where said master Rx clock signal is frequency locked to said Slave Tx clock signal (figure 1 lateral input block 60 column 4 lines 24); (c) a first controllable delay element for generating said Slave Tx clock signal from said Slave Rx clock signal (figure 1 block 65 column 16 lines 5-29); the communication link further comprising a decision processor responsive to said metric processor for changing a delay value of said controllable delay element so as to maximize the metric signal (figure 1 block 65 column 16 lines 5-29 figure 6 column 22 lines 8-26 figure 27 and figure 28 blocks 1512 and 467).

As per claim 4 Rakib discloses a second controllable delay between the Master Rx clock signal and the analog-to-digital converter and responsive to said decision processor, and the decision processor delays the Slave Tx clock signal and the sample time Ts independently to maximize the metric signal (figure 1 block 32 column 4 lines 34-35).

As per claim 5 Rakib discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, the bi-directional communication link (figure 1 block 32 column 4 lines 11-40); comprising: a metric processor for each master that produces a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (column 4 lines 41-46, figure 27 and figure 28 block 467); and a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to maximize the metric signal (figure 1 block 76 column 4 lines 36-38).

As per claim 8 Rakib discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, where the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, said bi-directional communication link comprising (figure 1 block 32 column 4 lines 11-40) a metric processor for each master that produces a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (column 4 lines 41-46, figure 27 and figure 28 block 467); and a decision processor responsive to said metric processor for

shifting said sample time Ts relative to the Master Tx clock so as to maximize the metric signal (figure 1 block 76 column 4 lines 36-38).

As per claim 11 Rakib discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, where the master receives a periodic noise burst comprising crosstalk from masters of adjacent channels and echoes of itself, the bidirectional communication link comprising (figure 1 block 32 column 4 lines 11-40 column 29 line 17 to column 30 line 3 and column 84 line 38 to column 85 line 22) a metric processor for each master that produces a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (column 4 lines 41-46, figure 27 and figure 28 block 467); and a decision processor responsive to said metric processor for shifting said sample time Ts relative to the Master Tx clock so as to maximize the metric signal (figure 1 block 76 column 4 lines 36-38).

As per claim 14 Rakib discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, where the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, where the master receives a

periodic noise burst comprising crosstalk from masters of adjacent channels and echoes of itself, the bidirectional communication link comprising (figure 1 block 32 column 4 lines 11-40 column 29 line 17 to column 30 line 3 and column 84 line 38 to column 85 line 22) a metric processor for each master that produces a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (column 4 lines 41-46, figure 27 and figure 28 block 467); and a decision processor responsive to said metric processor for shifting said sample time Ts relative to the Master Tx clock so as to maximize the metric signal (figure 1 block 76 column 4 lines 36-38).

As per claims 19, 25 and 27-30 Rakib discloses that the metric processor comprises a processor for computing the proportion of samples of the signal received by the master falling within the allowed amplitude levels relative to those that fall outside of the allowed amplitude levels (column 4 lines 41-46, figure 27 and figure 28 blocks 1512 and 467).

As per claim 20 Rakib discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, where the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, where the master receives a periodic noise burst comprising crosstalk from masters of adjacent channels and echoes of itself, a method of reducing the effects of the cross-talk and echo noise burst

on the signal received by each master, comprising (figure 1 block 32 column 4 lines 11-40 column 29 line 17 to column 30 line 3 and column 84 line 38 to column 85 line 22) for each master, producing a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (column 4 lines 41-46, figure 27 and figure 28 block 467); and in response to said metric signal shifting said sample time Ts relative to the Master Tx clock so as to reduce the effects of the noise burst on the received signal and increasing the metric signal (figure 1 block 76 column 4 lines 36-38).

As per claim 23 Rakib discloses that the shifting comprises the step of changing a delay between the Slave Rx cock and the Slave Tx clock (figure 1 block 65 column 16 lines 5-29).

Claims 1, 4-5, 8, 11, 14, 19-20, 23, 25, and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Trans (US 6377640).

As per claim 1 Trans discloses a bi-directional communication having plural channels, each of said channels comprising: a master connected at a near end of a channel and a slave connected at an opposite end of channel (figures 8-1, 8-2 and 8A column 14 lines 1-7); the master comprising: (a) a transmitter coupled to channel and having a master Tx clock signal (figure 3 transmitter section figure 10 column 14 line 10); (b) receiver coupled to the channel and comprising (figure 3 receiver section figure 10 column 14 line 10): i) an analog-to-digital converter that periodically samples at a sampling time Ts (figure 3 analog section 34 and digital section 32 figure 34 block 22 column 59 line 51); ii) a clock recovery circuit that signal embedded generates a master

Rx signal received from the channel (figure 3 block 355, figure 8A block 311 column 14 line 30); iii) a metric processor connected to an output of said analog-to-digital converter that produces a metric signal reflective of amplitude differences between the received signal and allowed amplitude levels of the received signal (figure 4 block 57 column 42 lines 33-65); the slave comprising: (a) a receiver coupled to the channel and comprising a clock recovery circuit for generating a Slave Rx clock from the signal received from the master (figure 3 receiver section figure 10 column 14 line 10); (b) a transmitter coupled to the channel and having a Slave Tx clock signal, whereby said master Rx clock signal is frequency locked to said Slave Tx clock signal (figure 3 transmitter section figure 10 column 14 line 10); (c) a controllable delay element for generating said Slave Tx clock signal from said Slave Rx clock signal (figure 34 column 64 line 32); the communication link further comprising a decision processor responsive to said metric processor for changing a delay value of said controllable delay element so as to maximize the metric signal (figure 5a block M212 column 16 lines 37-38).

As per claim 4 Trans discloses a second controllable delay between the Master Rx clock signal and the analog-to-digital converter and responsive to said decision processor, and the decision processor delays the Slave Tx clock signal and the sample time Ts independently to maximize the metric signal (figure 5a column 34 lines 24-28).

As per claim 5 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the

Slave Rx clock, the bi-directional communication link (figures 8-1, 8-2, 8A and 10C-2 column 14 lines 1-7); comprising: a metric processor for each master that produces a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (figure 4 block 57 column 42 lines 33-65); and a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to maximize the metric signal (figure 5a block M212 column 16 lines 37-38).

As per claim 8 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, said bi-directional communication link comprising (figures 8-1, 8-2, 8A and 10C-2 column 14 lines 1-7) a metric processor for each master that produces a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (figure 4 block 57 column 42 lines 33-65); and a decision processor responsive to said metric processor for shifting said sample time Ts relative to the Master Tx clock so as to maximize the metric signal (figure 5a column 34 lines 24-28).

As per claim 11 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels,

each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock wherein each master receives a periodic noise burst comprising cross-talk (figures 1B-1 1B-2, 1B-3, 5b and 5d column 35 line 47) from masters of adjacent channels and echoes of itself, said bi-directional communication link comprising: a metric processor for each master that produces a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (figure 4 block 57 column 42 lines 33-65); and a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal (figure 5a column 34 lines 24-28).

As per claim 14 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk (figures 1B-1 1B-2, 1B-3, 5b and 5d column 35 line 47) from masters of adjacent channels and echoes (figure 10C-2) of itself, said bi-directional communication link comprising: a metric processor for each master that produces a metric signal reflective of amplitude differences between a

signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (figure 4 block 57 column 42 lines 33-65); and a decision processor responsive said for shifting said sample time Ts relative the Tx clock so as to reduce the effects of the noise and thereby increase the metric (figure 5a column 34 lines 24-28).

As per claims 19, 25 and 27-30 Trans discloses that the metric processor comprises a processor for computing the proportion of samples of the signal received by the master falling within the allowed amplitude levels relative to those that fall outside of the allowed amplitude levels (figure 4 block 57 column 42 lines 33-65).

As per claim 20 Trans (US 6377640) discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency (figure 5a column 34 lines 24-28) locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk (figures 1B-1 1B-2, 1B-3, 5b and 5d column 35 line 47) from masters of adjacent channels and echoes of itself (figure 10C-3), a method of reducing the effects of the cross-talk and echo noise burst on the signal received by each master, comprising: for each master, producing a metric signal reflective of amplitude differences between a signal received by the master from the corresponding slave and allowed amplitude levels of the received signal (figure 4 block 57 column 42 lines 33-

65); and in response to said metric signal, shifting said sample time Ts relative to the Master Tx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal (figure 5a column 34 lines 24-28).

As per claim 23 Trans discloses that the shifting comprises the step of changing a delay between the Slave Rx cock and the Slave Tx clock (figure 5a column 34 lines 24-28).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
05-03-2005

M. Gh

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER